

FIG. 1

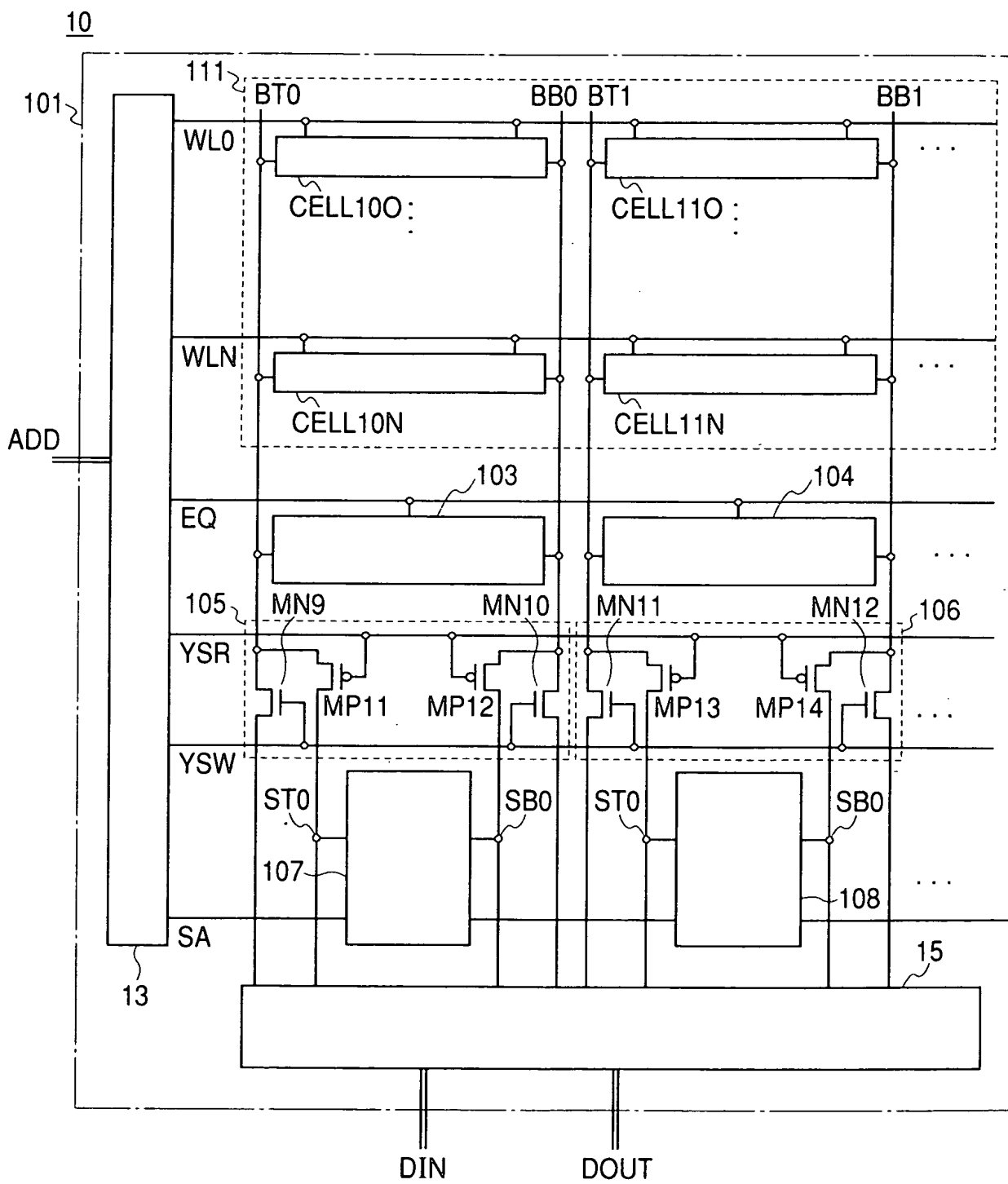


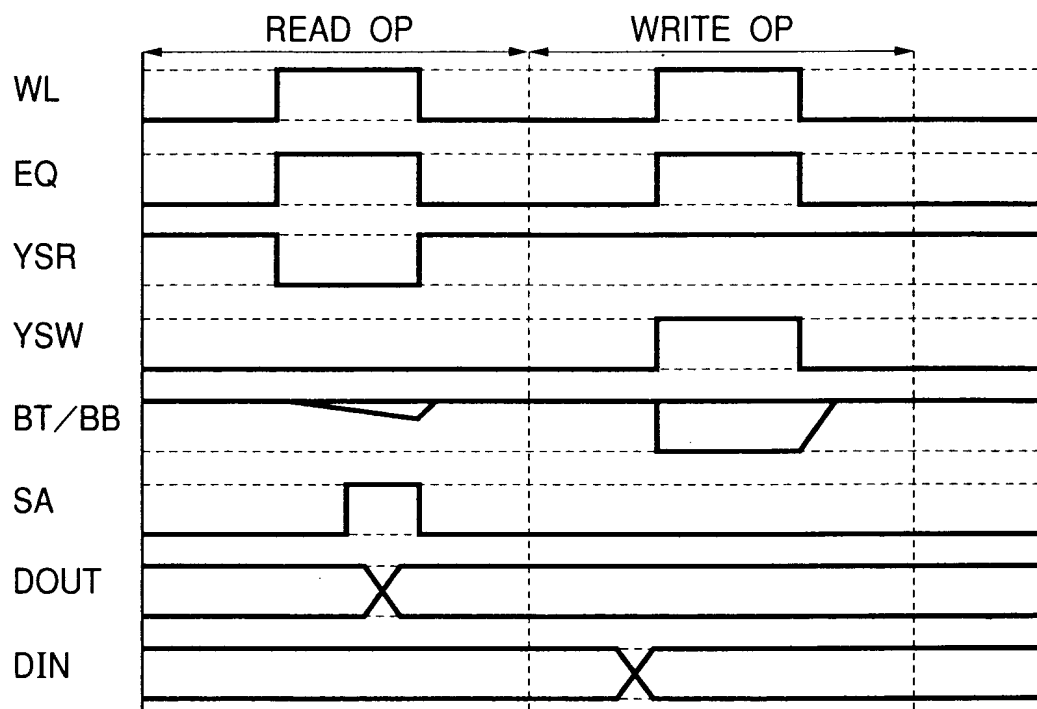
FIG. 2

FIG. 3

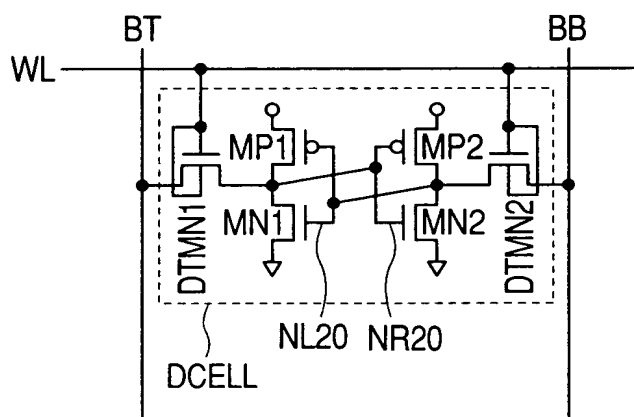


FIG. 4

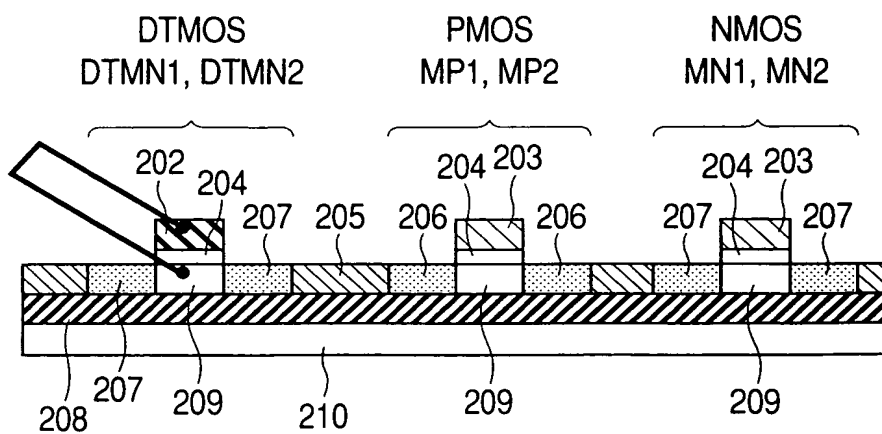


FIG. 5

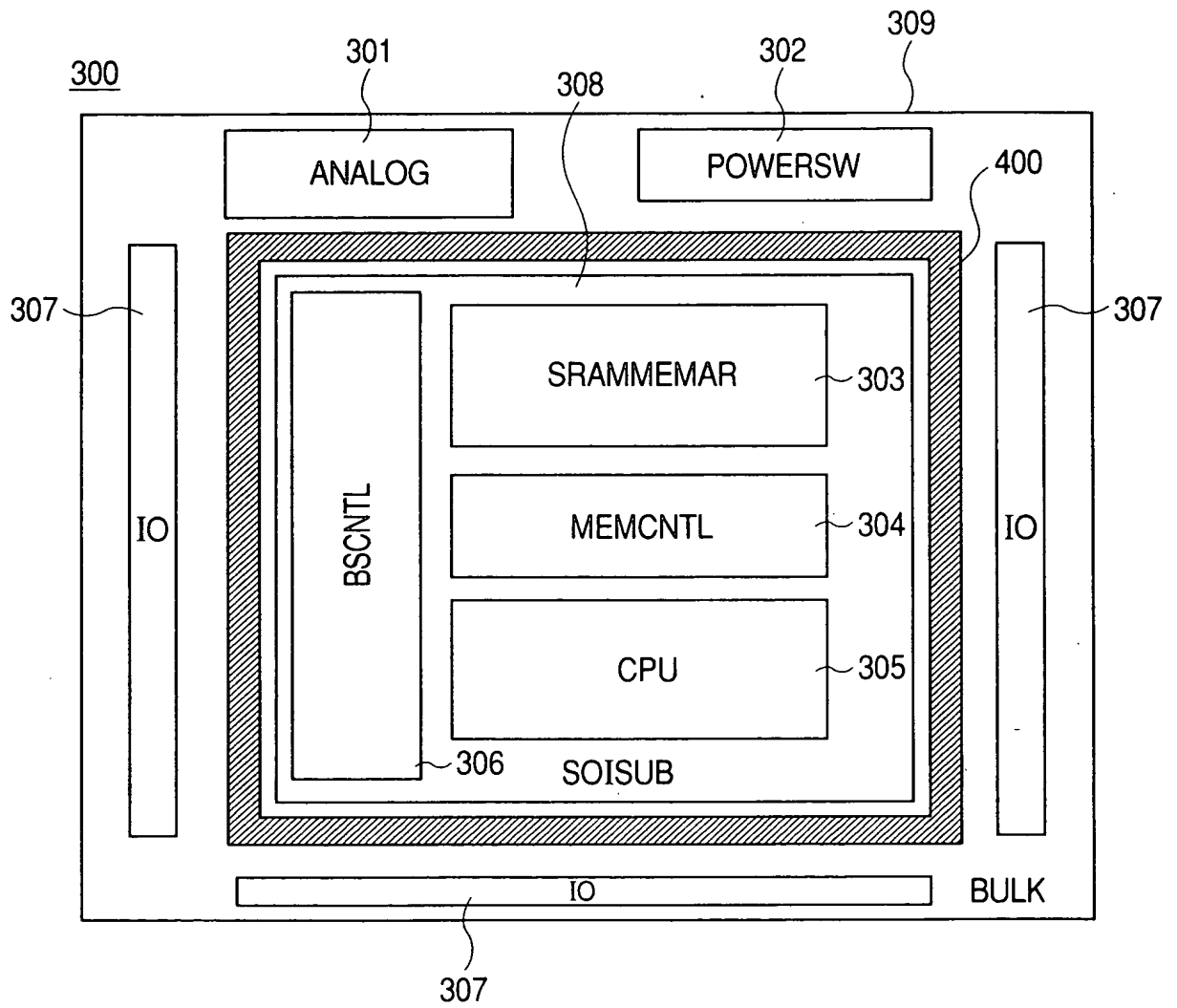


FIG. 6

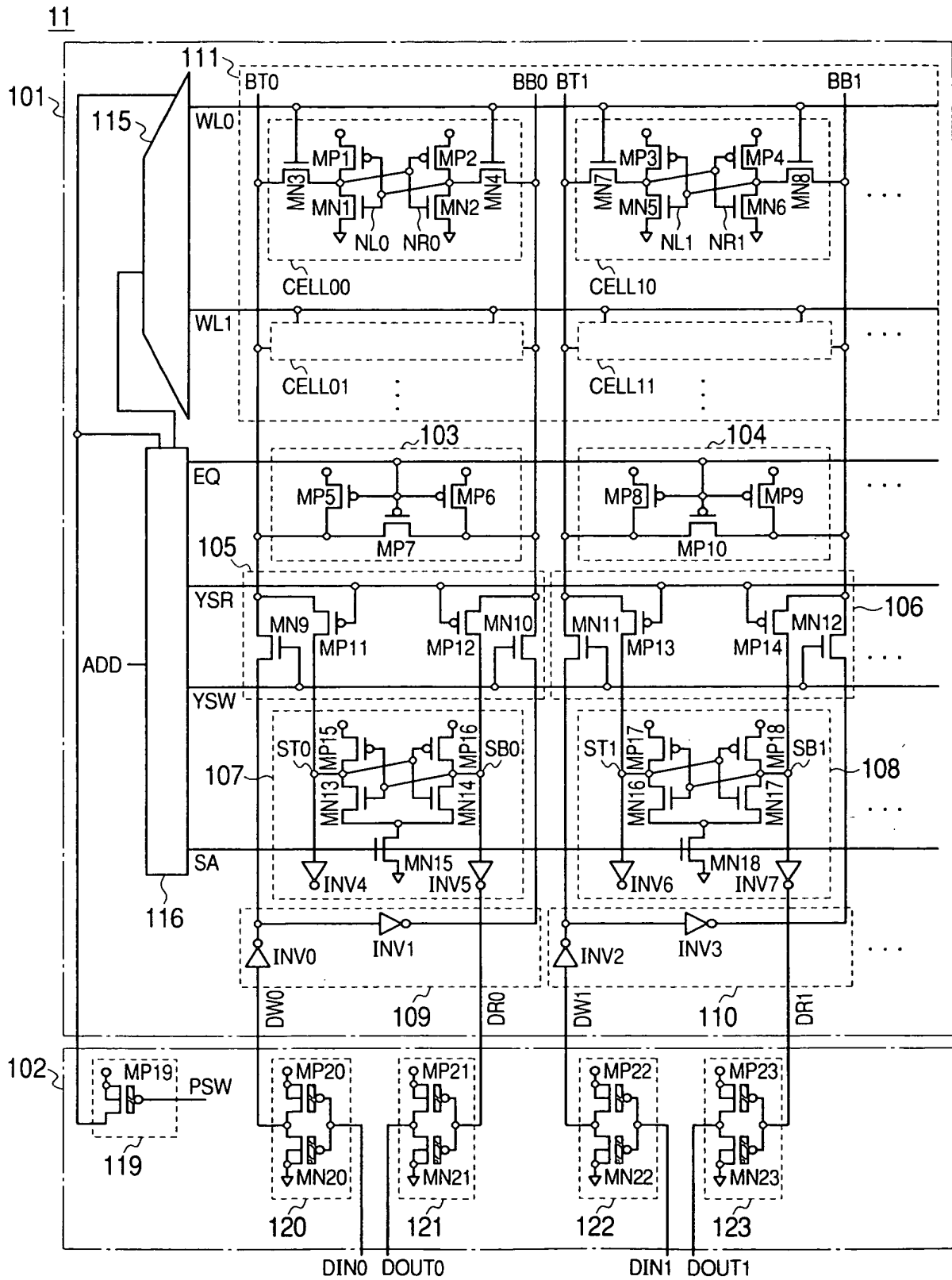


FIG. 8

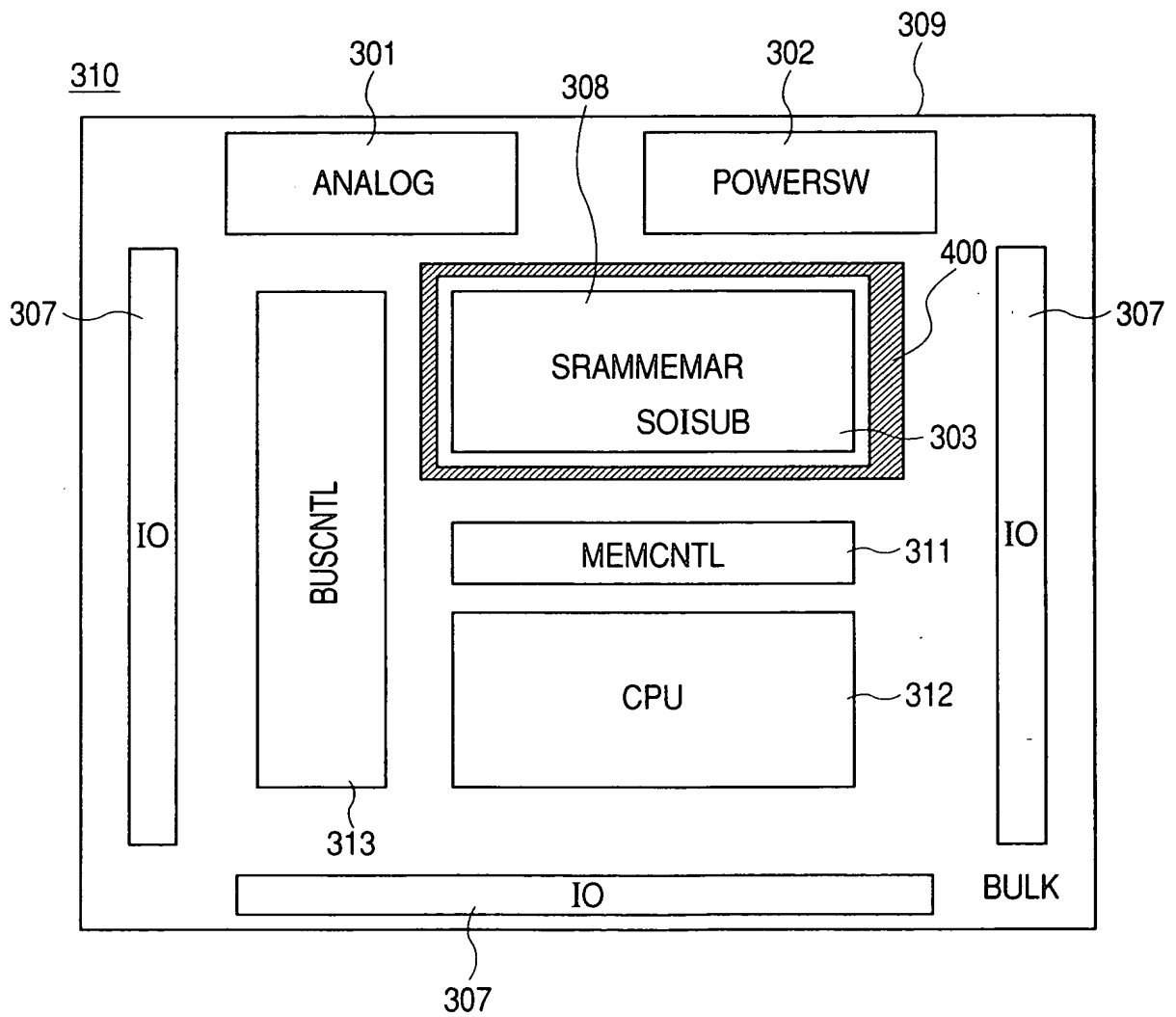


FIG. 9

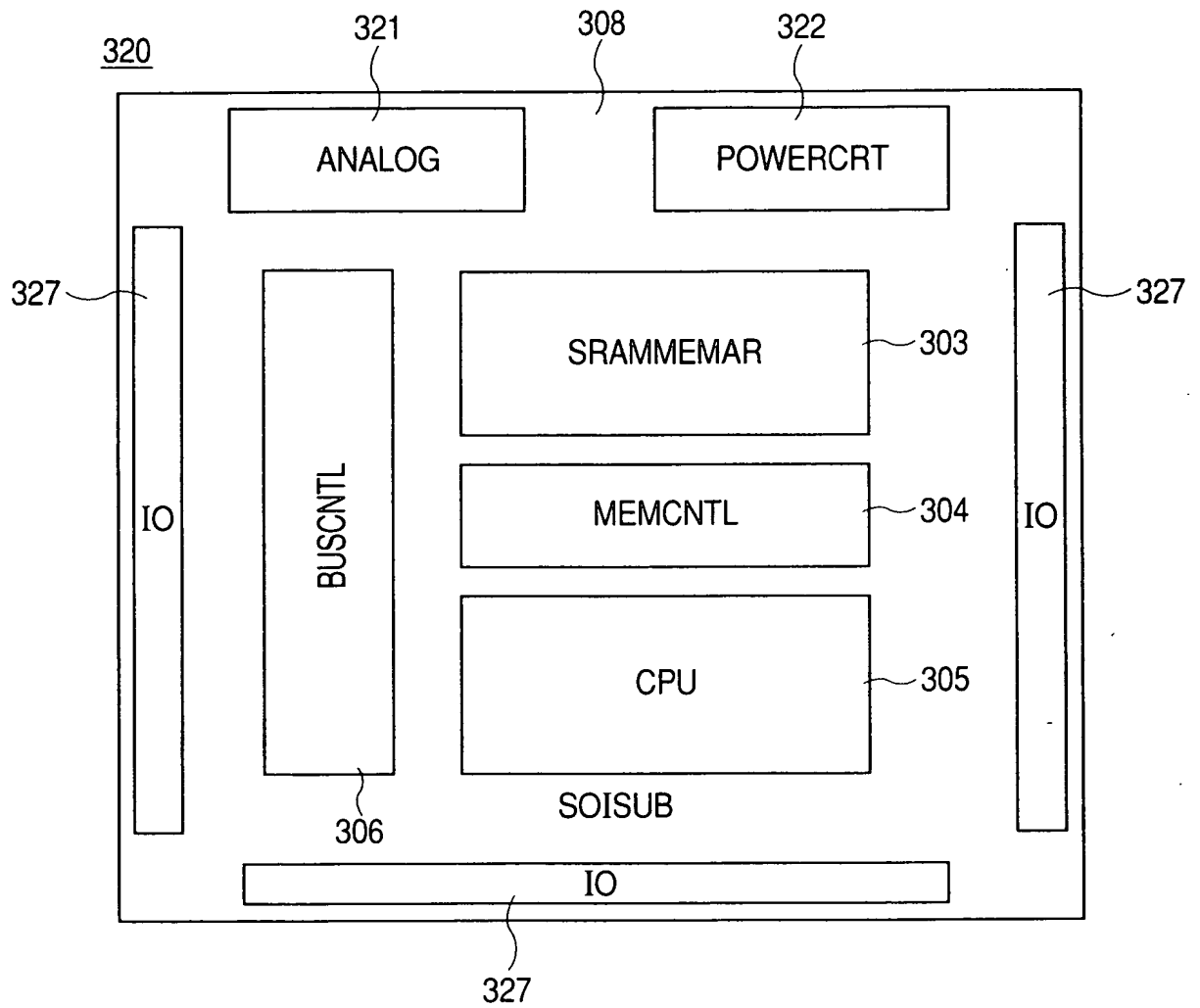


FIG. 10

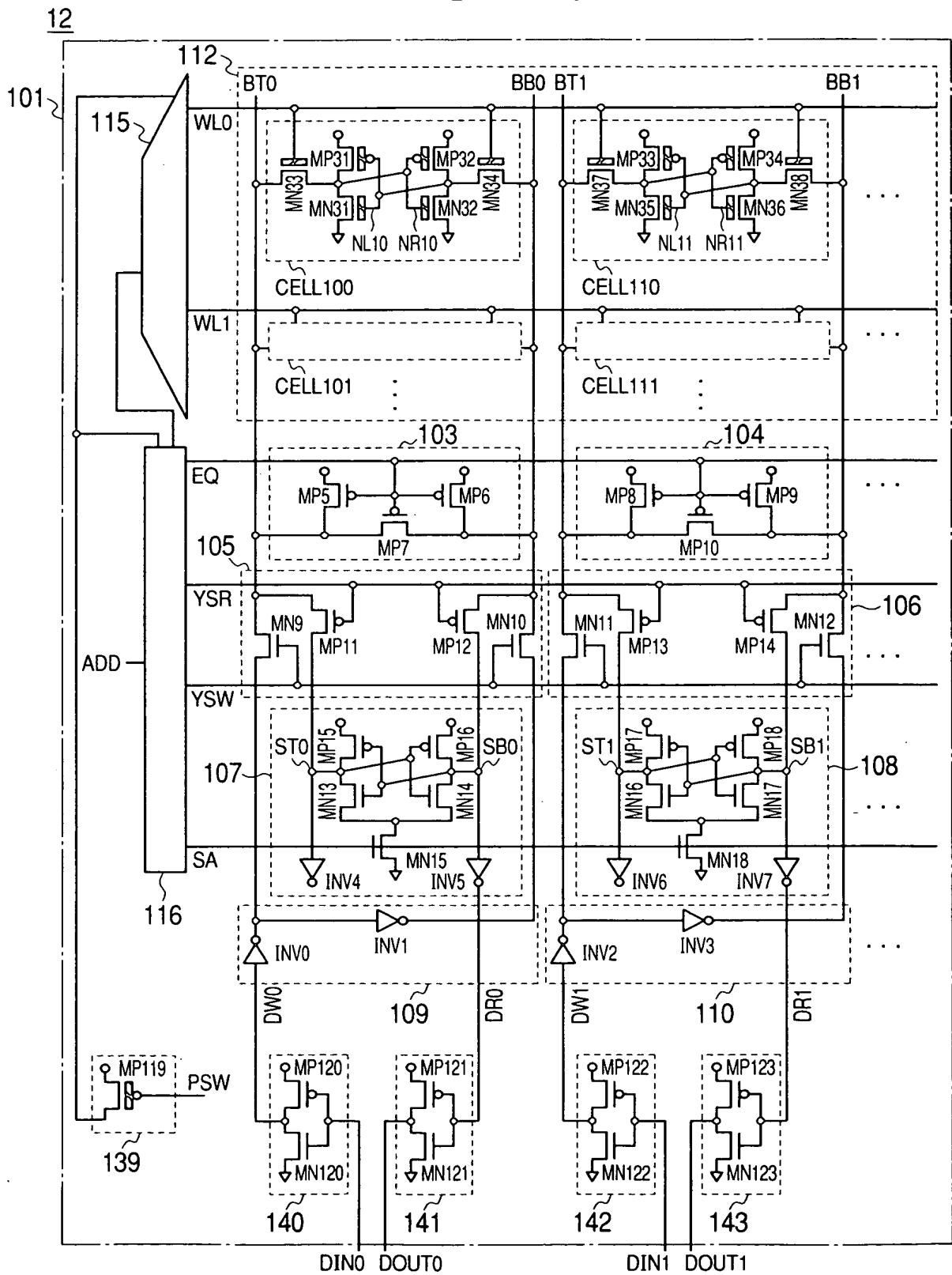


FIG. 11

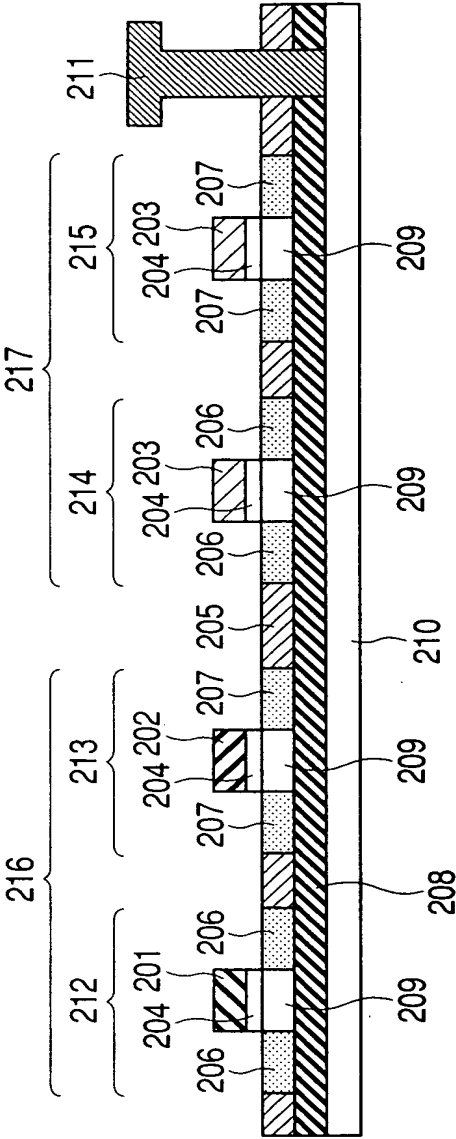


FIG. 12

SOISUB		HIGHSPEED					STANDARD				
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	SOI	SiGe	P	O	-0.3	SOI	SiGe	P	3V	-0.3
	NMISFET	SOI	SiGe	P	O	0.3	SOI	SiGe	P	3V	0.3
SRAM	PMISFET	SOI	SiGe	P	O	-0.3	SOI	Poly-Si	N	3V	-1.0
	NMISFET	SOI	SiGe	P	O	0.3	SOI	Poly-Si	P	3V	0.6

SOISUB		STANDARD						LOWPOWER			
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	SOI	VERTICALMOS				SOI	Poly-Si	N	X	-0.8
	NMISFET	SOI	Poly-Si	P	3V	0.6	SOI	Poly-Si	P	X	0.8
	PMISFET	SOI	VERTICALMOS				SOI	Poly-Si	N	X	-0.8
SRAM	NMISFET	SOI	Poly-Si	P	3V	0.6	SOI	Poly-Si	P	X	0.8

HYBRIDSUB		HIGHSPEED					STANDARD				
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	SOI	SiGe	P	O	-0.3	SOI	SiGe	P	3V	-0.3
	NMISFET	SOI	SiGe	P	O	0.3	SOI	SiGe	P	3V	0.3
SRAM	PMISFET	SOI	SiGe	P	O	-0.3	SOI	Poly-Si	N	3V	-1.0
	NMISFET	SOI	SiGe	P	O	0.3	SOI	Poly-Si	P	3V	0.6
IO/Analog/SW		BULK	-	-	-	ANY	BULK	-	-	-	ANY

HYBRIDSUB		STANDARD					LOWPOWER				
		SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]	SUB	GATEMAT	GATEIMP	SOIVBB	VT[V]
LOGIC	PMISFET	BULK	-	-	-	ANY	BULK	-	-	-	ANY
	NMISFET	BULK	-	-	-	ANY	BULK	-	-	-	ANY
SRAM	PMISFET	SOI	VERTICALMOS				SOI	Poly-Si	N	X	-0.8
	NMISFET	SOI	SiGe	P	NONE	0.5	SOI	Poly-Si	P	X	0.8
IO/Analog/SW		BULK	-	-	-	ANY	BULK	-	-	-	ANY

FIG. 13

		HIGH SPEED 300MHz~ Vdd<1.0V	STANDARD 100MHz~300MHz Vdd≒1.0V	LOW POWER ~100MHz Vdd>1.0V
Logic	PMOSVT	-0.3V~-0.1V	-0.4V~-0.2V	-0.9V~-0.7V
	NMOSVT	0.1V~0.3V	0.2V~0.4V	0.7V~0.9V
SRAM	PMOSVT	-0.5V~-0.3V	-1.0V~-0.8V	-0.9V~-0.7V
	NMOSVT	0.2V~0.4V	0.4V~0.6V	0.7V~0.9V

FIG. 14

GATE MAT	Poly-Si		SiGe	
GATE IMP	P	N	P	N
PMOS Vto	+0.2V	-0.8V	-0.1V	-0.8V
NMOS Vto	+0.8V	-0.2V	0.5V	-0.2V

FIG. 15

	ELE	BULK	FD-SOI
V _{bbb}	L _{Vth} MOS + V _{BBBCRT}	EFFECT IS LOW UNDER 100nm	EFFECT EVEN UNDER 100nm
V _{bbf}	H _{Vth} MOS + V _{BBFCRT}	EFFECT IS LOW AT HIGH TEMPERATURE LEAK CURRENT IS LARGE	HIGH TEMPERATURE OPERATION AVAILABLE, SMALL LEAK CURRENT, ON CURRENT LARGE
V _{bbact}	V _{th} MOS + M _N TCRT + V _L TCRT	WITH ABOVE REASONS, CORRECTIONS FOR V _{TH} DISPERSION IS NOT EFFECTIVE	EFFECTIVE UNDER 100nm & HIGH TEMPERATURE

FIG. 17

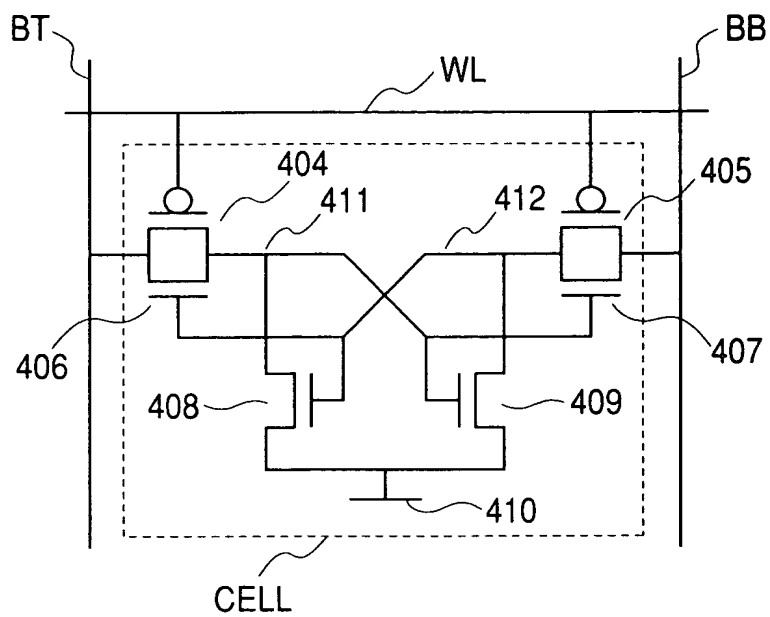


FIG. 18

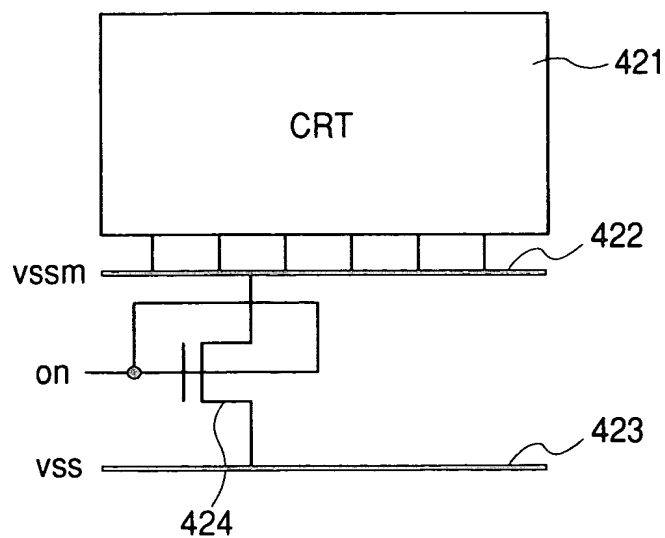


FIG. 19